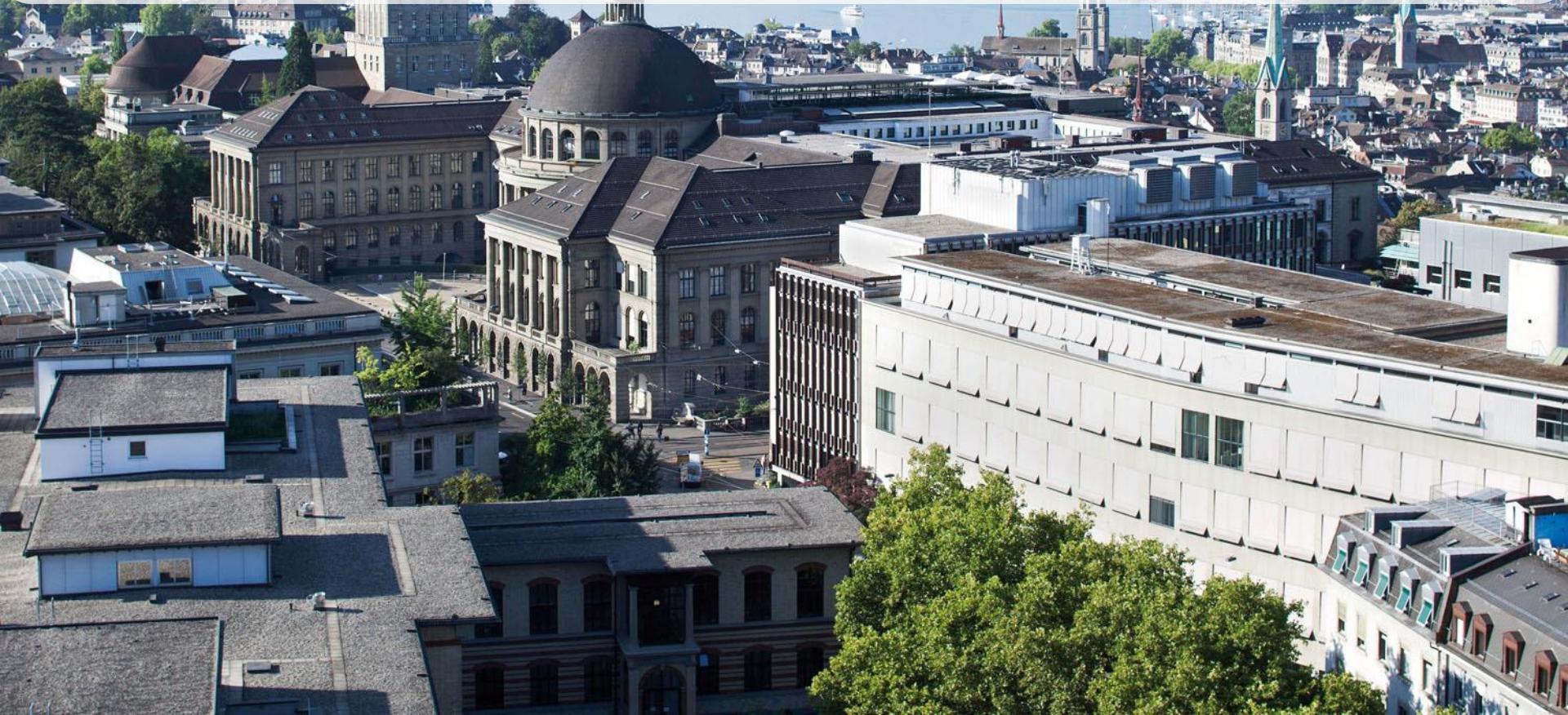


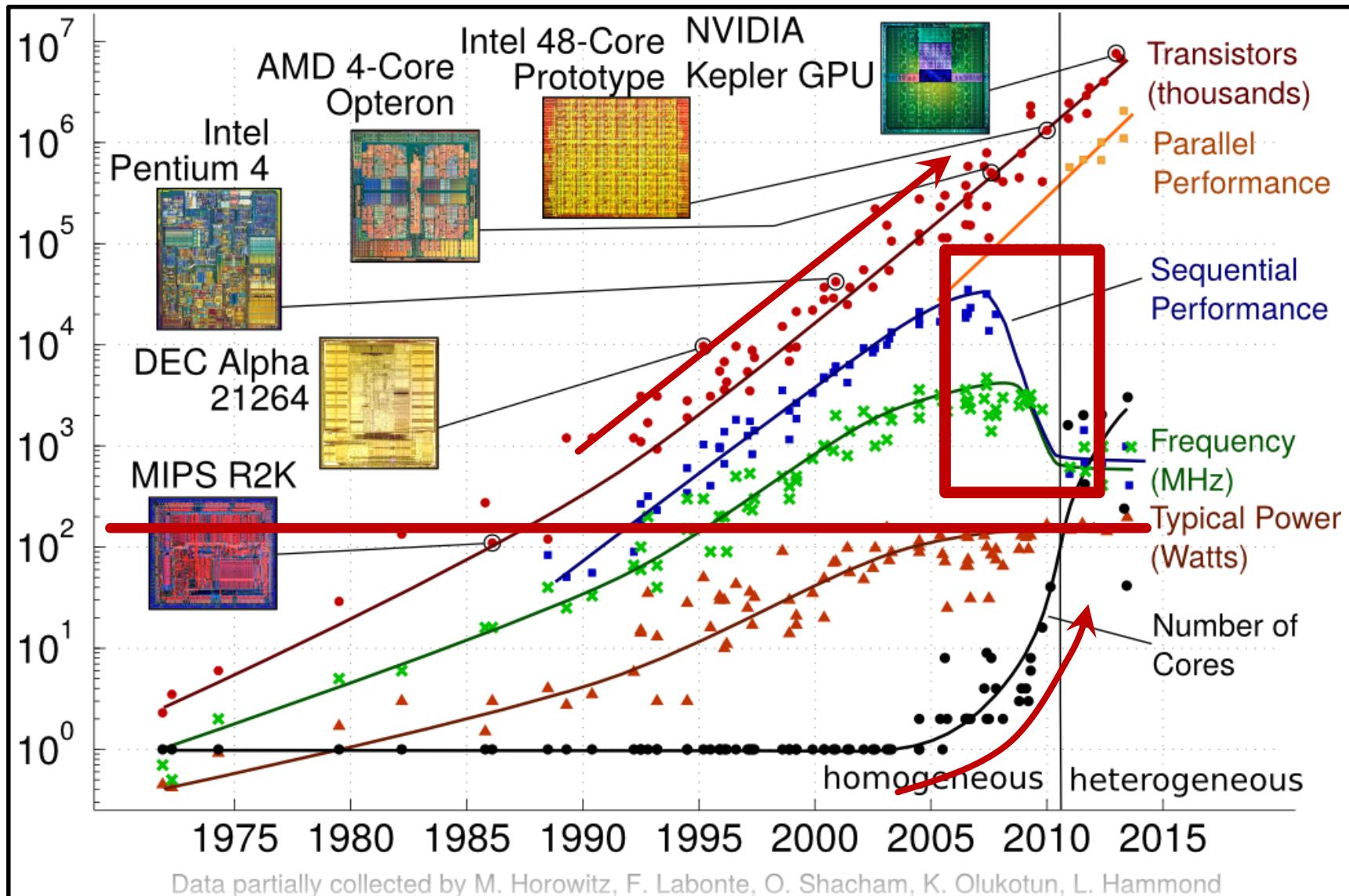
**TORSTEN HOEFLER**

DEPARTMENT OF COMPUTER SCIENCE

ETH ZÜRICH

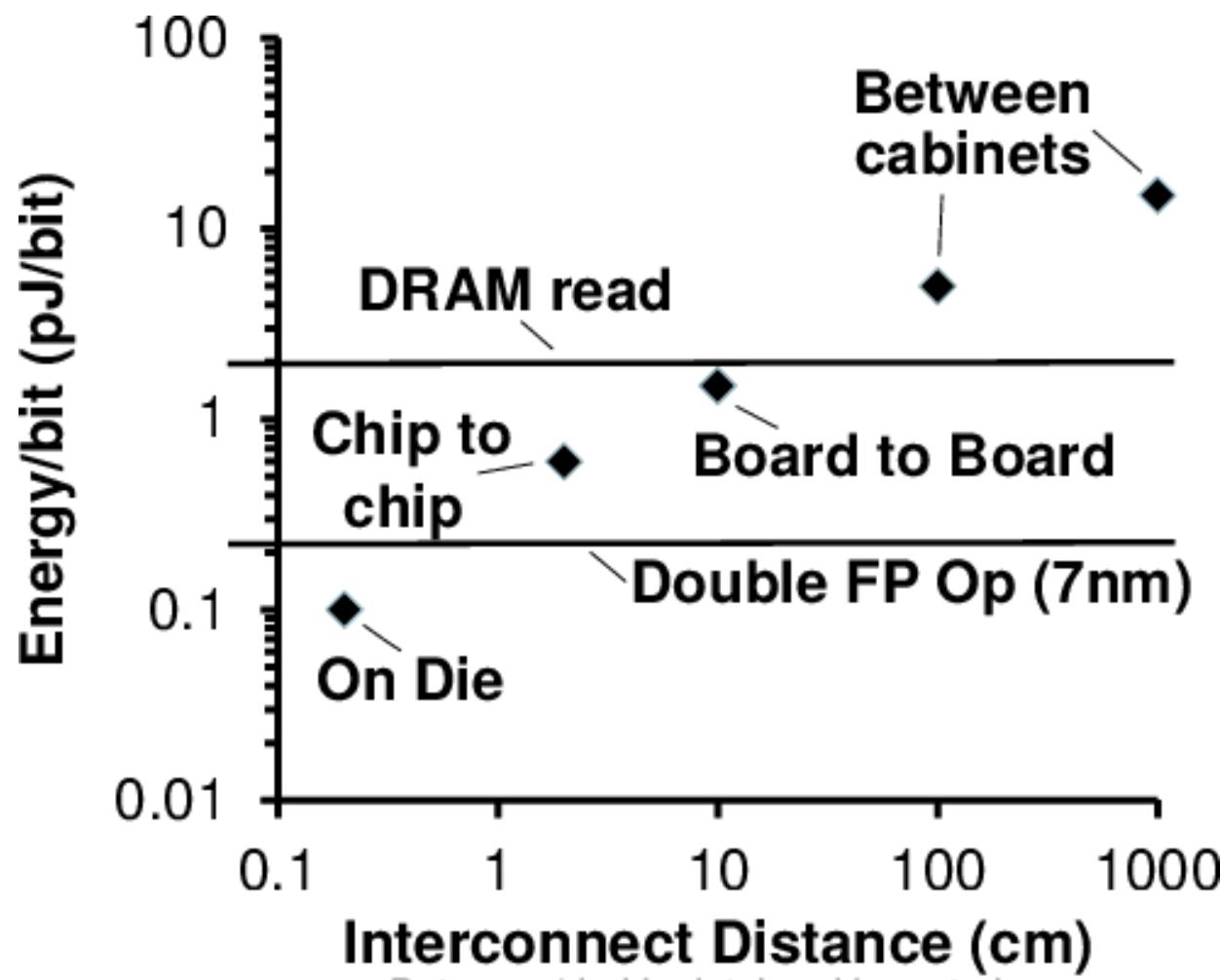
# ROSS 2016 – Panel: The Role of System Software in the HPC Accelerator Space





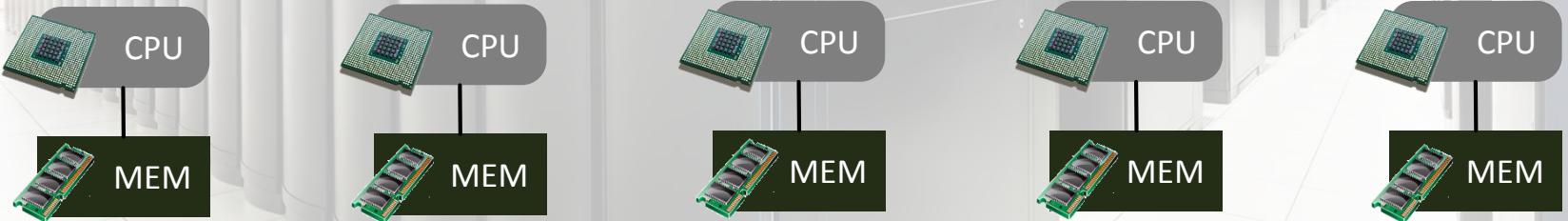
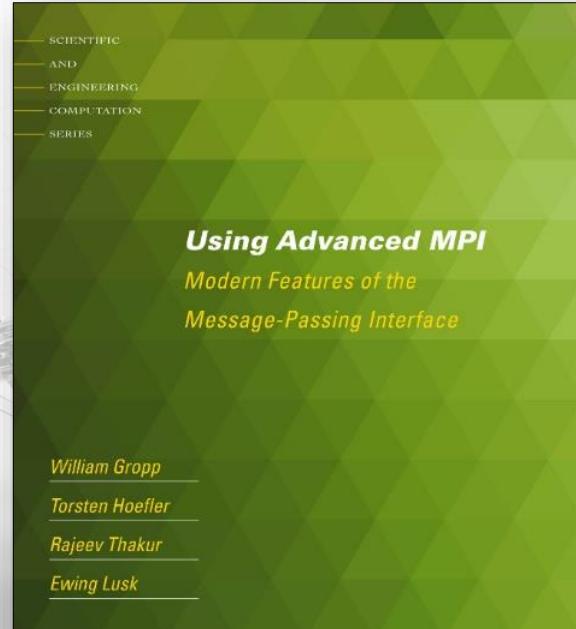
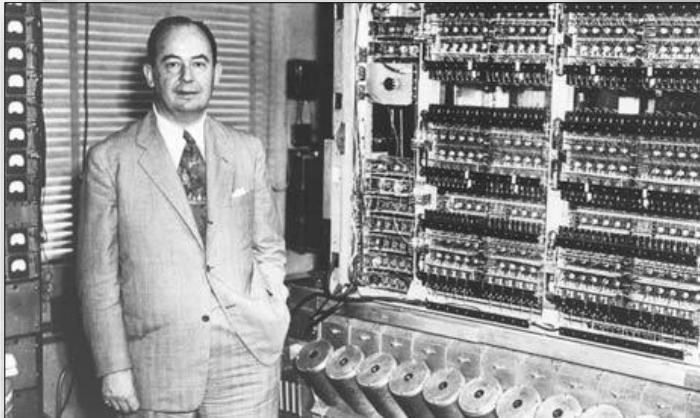
So more parallelism but what is the cost?

# Energy Consumption Trends in Computing

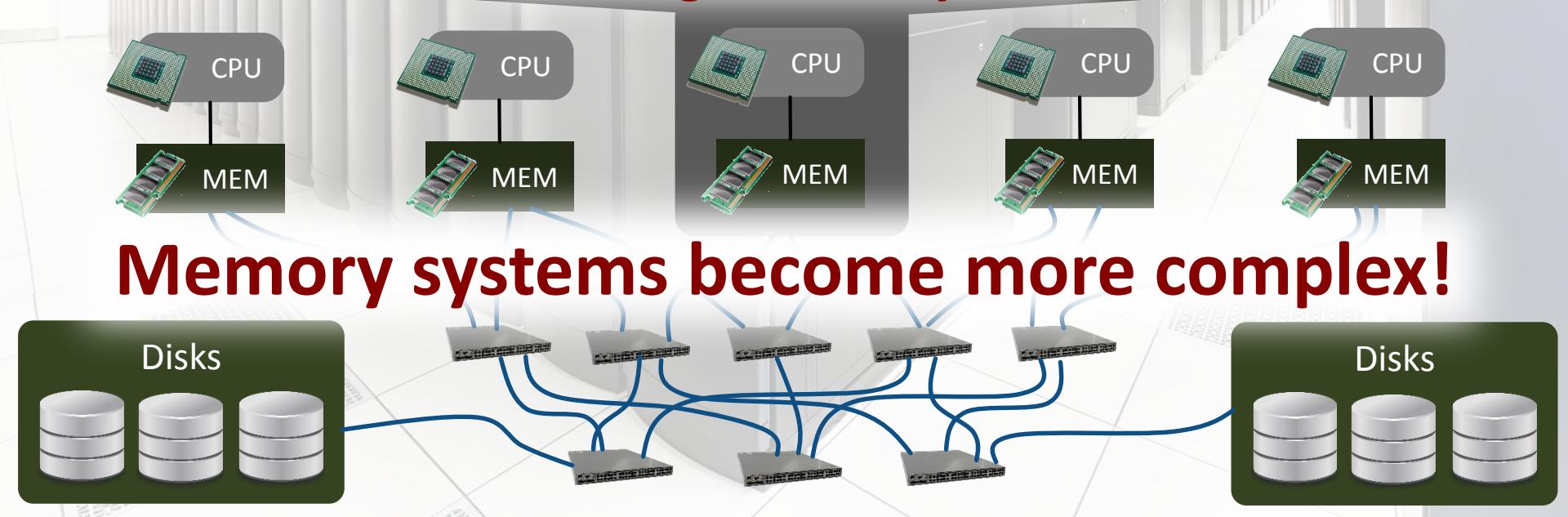
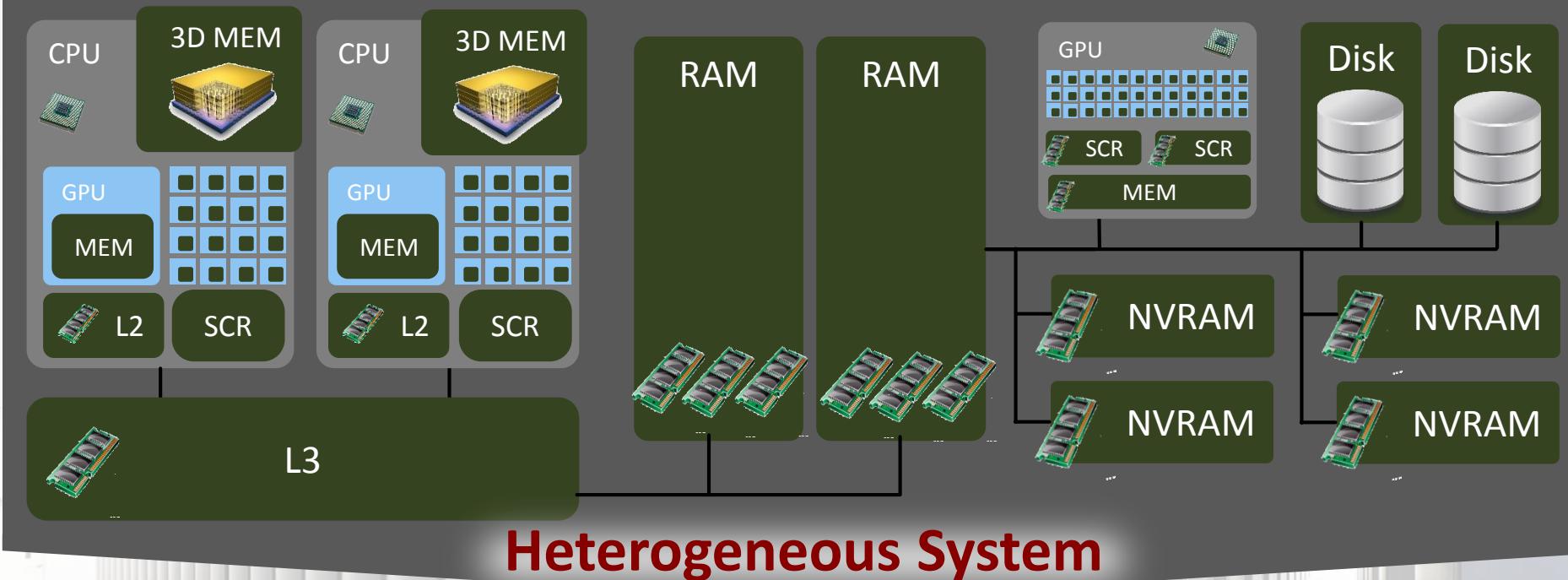


Data provided by Intel and Lee et al.

**Data movement is the major challenge!**

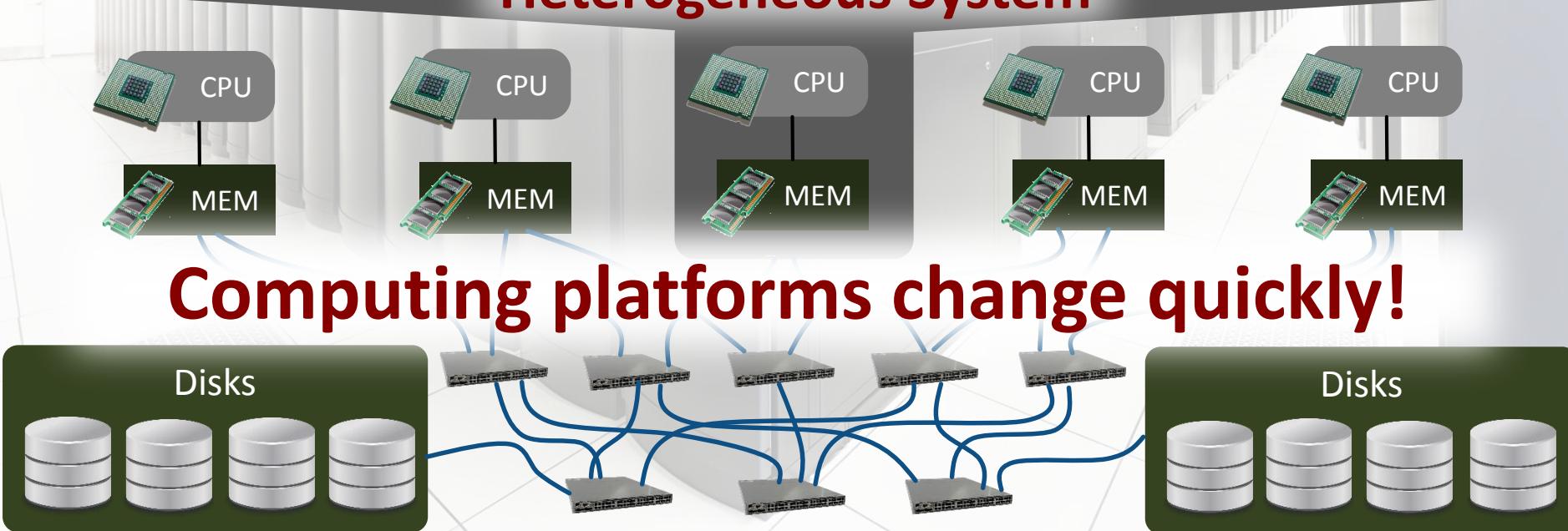
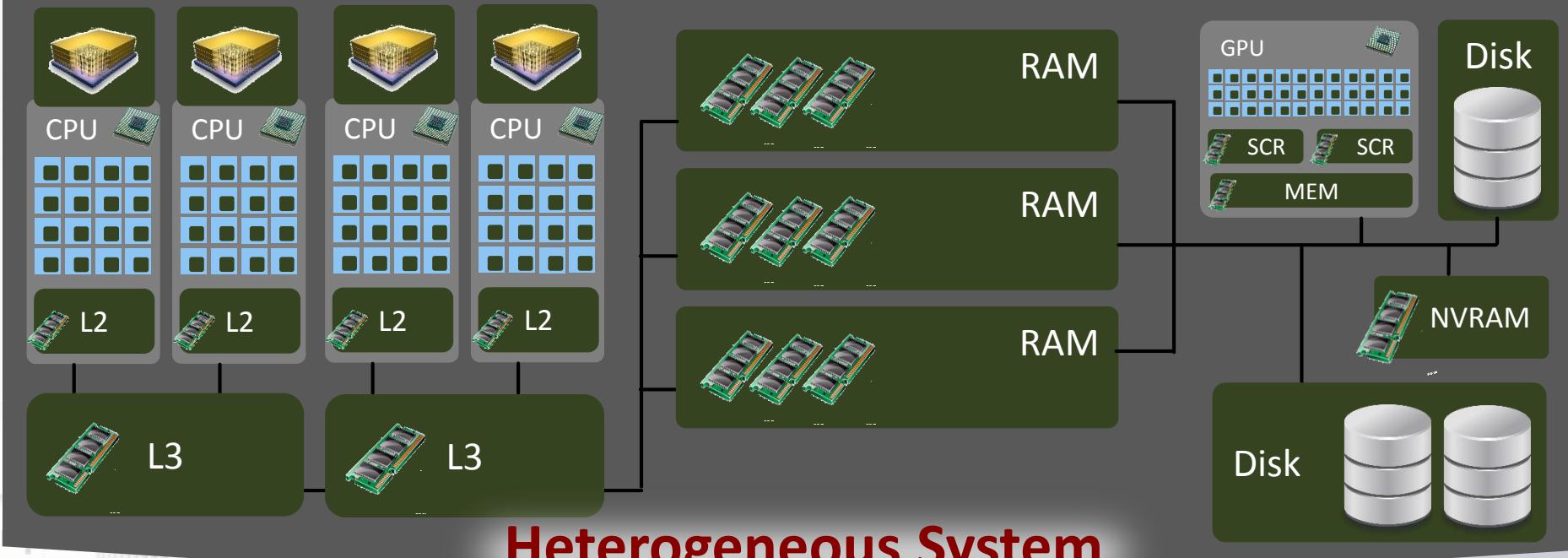


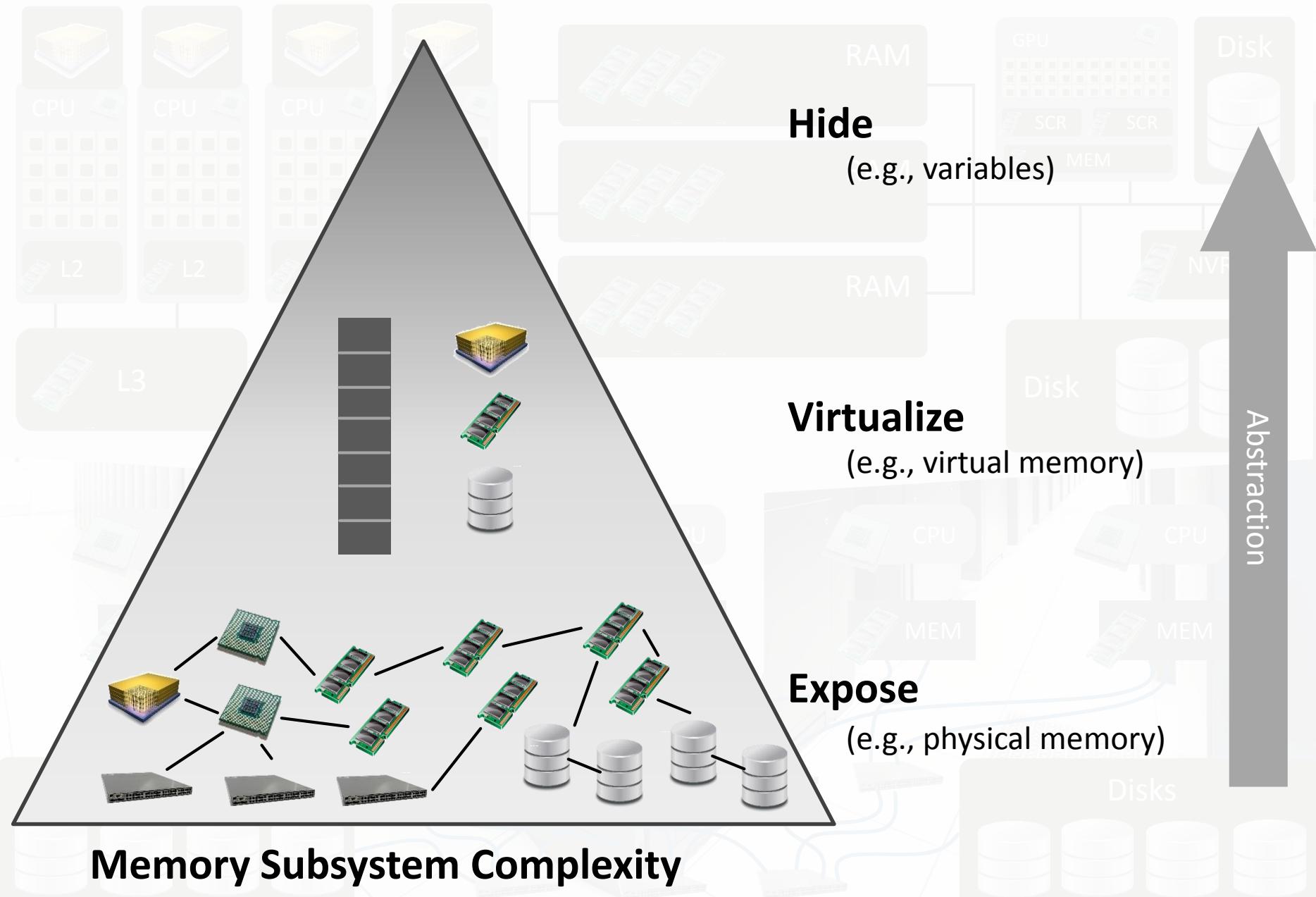
**Well, managing data is the major challenge!**



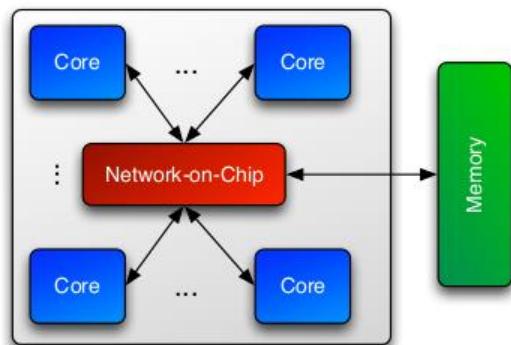
Memory systems become more complex!



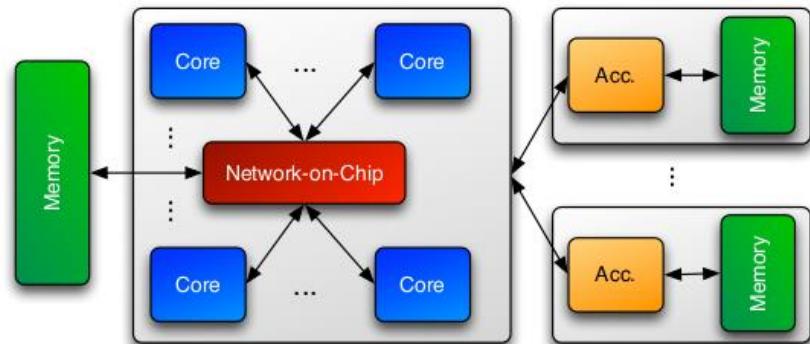




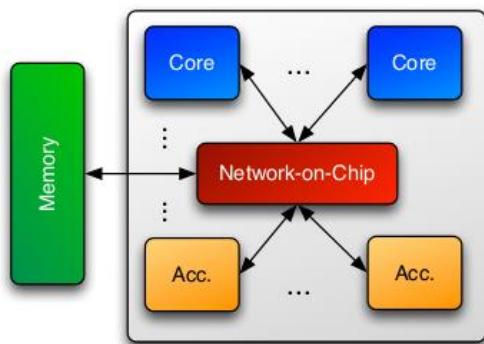
# Likely Future Abstract Machine Models (2014)



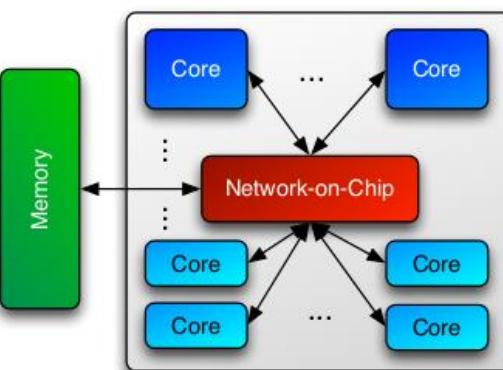
Homogeneous Many-Core Model



Multi-Core CPU + Discrete Accelerator



Integrated CPU + Accelerators



Heterogeneous Multicore

# So we'll all have to deal with accelerators?

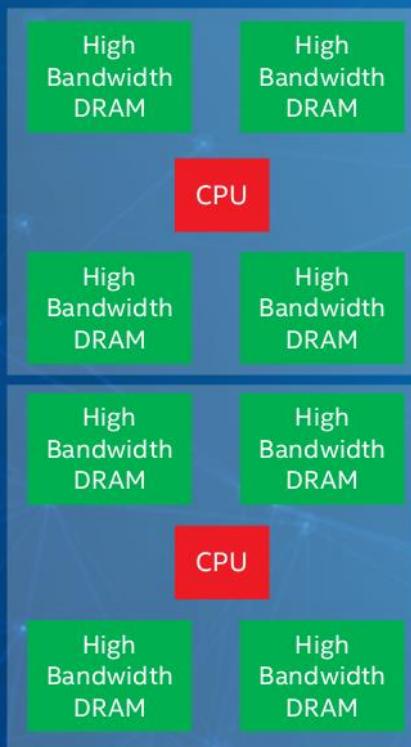
- If we mean specialized logic: probably yes!
- Remember this guy?



- Do we need system software for him?

# Intel's View (Slide from Alan Gara, 2015)

## Repartitioning of the design

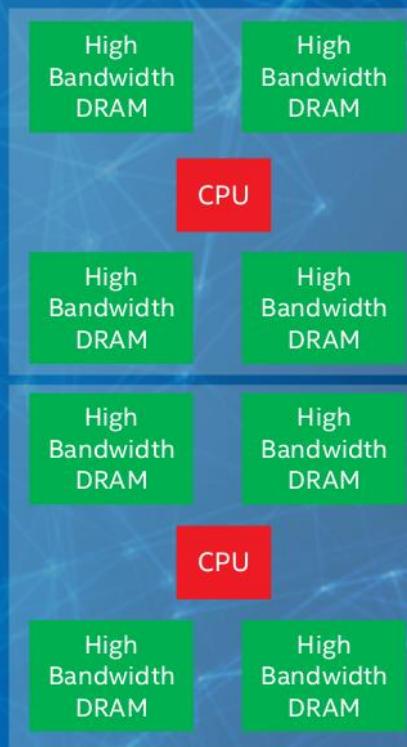


By repartitioning the way we build nodes...

We can have all DRAM integrated into nodes allowing for 15x more memory BW.

The memory capacity per core does not need to be sacrificed (any more than with traditional DRAM)

The biggest hurdle is to recognize that adding cores adds power which is not general purpose performance as other resources can not be similarly increased



Memory-centric CPU design perspective from Intel (cf. Intel Xeon Phi KNC/KNL)

# And now to the battle of Yamazaki (reenacted)



source: wikipedia



# The fighters, aehem panelists